DURGAPUR INSTITUTE OF ADVANCED TECHNOLOGY AND MANAGEMENT

(Affiliated to MAKAUT and recognized by AICTE, New Delhi)

Subject Code: IT 502 Subject Name: Computer Architecture

Semester : V Year: 3RD Session : 2018

Branch Name: Information Technology Faculty Name: Sulekha Nandi
Assistant Professor
IT Department

Syllabus

Module – 1: [12 L]

Introduction: Review of basic computer architecture (Revisited), Quantitative techniques in computer design, measuring andreporting performance. Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards and structural hazards,techniques for handling hazards.Exception handling. Pipeline optimization techniques; Compiler techniques for improving performance.

Module – 2: [8L]
Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques forreducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.

Module – 3: [6L]
Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, superpipelined and VLIW processorarchitectures. Array and vector processors.

Module – 4: [12 L]
Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared- memory architecture: synchronization,memory consistency, interconnection networks. Distributed shared-memory architecture. Cluster computers. Non von Neumann architectures: data flow computers, reduction computer architectures, systolic architectures.

TEXT BOOK:

1. Computer Architecture and Parallel Processing, Kai Hwang, Fayé A. Briggs
2. Computer system architecture -M. Morris Mano
3. Computer Architecture: A Quantitative Approach-John L. Hennessy, David A. Patterson

REFERENCE BOOK:

a) Advanced Computer ArchitectureBy Rajiv Chopra
b) Computer Arithmetic: Principles, Architecture, and Design- Kai Hwang
c) Computer Organization and Architecture: Designing for Performance-William Stallings

Course Outcomes:

(1) Review of basic computer architecture, Quantitative techniques in computer design, measuring and reporting performance.
(2) Classify different kinds of pipeline, pipeline hazards and suggesting suitable remedial techniques to handle the hazards. Discussing different kinds of parallel architectures (Flynn's Classification), types of Multiprocessor architectures (UMA, NUMA, COMA and NORMA), types of Inter connection (Bus,

Hypercube and Omega) network and Memory Consistency models. Explaining the concepts of Centralized shared memory architecture and Distributed shared memory architecture.
(3) Compute performance parameters of pipelines (Speed-up, Efficiency and Throughput) and deduce derivations to demonstrate the performance parameters when branching effect is introduced. Pipeline optimization techniques needs to be illustrated. Preparing numerical module based on pipeline concepts.
(4) Differentiate between different Memory technologies (Primary, Secondary and Cache) and helping students to compute different kinds of numerical based on the memory technologies.
(5) Collecting knowledge about Superscalar, Super pipelined and VLIW processor architectures, Array and vector processors. Constructing the concepts of ILP.
(6) Comparing different techniques of ILP (Loop Unrolling, Dynamic Scheduling and Software Pipelining) and concluding with concepts of Data Flow architecture, RISC, CISC and Systolic architecture

LESSION PLAN

Sr. No.	Day	Reference of the Syllabus	Remarks
1	Lecture 1	Introduction: Review of basic computer architecture.	
2	Lecture 2	Quantitative techniques in computer design, measuring andreporting performance.	
3	Lecture 3		
4	Lecture 4	Pipelining: Basic concepts	
5	Lecture 5	Instruction and arithmetic pipeline,	
6	Lecture 6		
7	Lecture 7	Data hazards, control hazards and structural hazards, techniques for handling hazards.	
8	Lecture 8		
9	Lecture 9		
10	Lecture 10	Pipeline optimization techniques;	
11	Lecture 11	Exception handling.	
12	Lecture 12	Compiler techniques for improving performance.	
13	Lecture 13	Hierarchical memory technology: Inclusion, Coherence and locality properties	
14	Lecture 14	Cache memory organizations	
15	Lecture 15		
16	Lecture 16	Techniques for reducing cache misses	
17	Lecture 17	Virtual memory organization	

18	Lecture 18		
19	Lecture 19	Mapping and management techniques,	
20	Lecture 20	Memory replacement policies.	
21	Lecture 21		
22	Lecture 22	Instruction-level parallelism: basic concepts, techniques for increasing ILP	
23	Lecture 23	Superscalar, superpipelined and VLIW processor architectures	
24	Lecture 24		
25	Lecture 25		
26	Lecture 26	Array and vector processors.	
27	Lecture 27	Multiprocessor architecture: taxonomy of parallel architectures;	,,
28	Lecture 28		
29	Lecture 29	Centralized shared- memory architecture: synchronization, memory consistency	
30	Lecture 30		
31	Lecture 31	Interconnection networks	
32	Lecture 32		
33	Lecture 33		
34	Lecture 34	Distributed shared-memory architecture. Cluster computers.	
35	Lecture 35	Non von Neumann architectures: data flow computers	
36	Lecture 36		
37	Lecture 37	Reduction computer architectures	
38	Lecture 38	Systolic architectures	

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Signature of HOD **Signature of the faculty**